Power Conditioning System with Cascaded H-Bridge Multilevel Converter – DC-link Voltage Balancing Method

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Keywords

«Multilevel converters», «Power conditioning», «Converter control», «DC-link voltage balancing»

Abstract

Multilevel converters have become an attractive choice for high voltage and high power applications. One of the most popular multilevel converter topologies is the cascaded H-bridge converter. Besides its simplicity this topology requires separate DC sources. In electric drive applications these DC sources are normally performed by multi-winding transformers with diode rectifiers. In STATCOM or PWM rectifiers there is no need to utilize multi-winding transformers but the DC-link is distributed. This feature can be exploited in the power conditioning system (PCS) with distributed energy storage e.g. supercapacitors. The paper focuses on the DC-link voltage balancing method in the multilevel cascaded H-bridge converter. This method is based on additional voltage components generated at the output of the cascaded H-bridge converter. It is assumed that the proposed method does not affect the AC-side currents of the PCS. Inserting the voltage components of fundamental frequency, together with AC-side currents, allows exchanging active power between the H-bridge converters and results in balancing the DC-link voltages. In the paper, balancing voltage components are distinguished into two types. The first components can balance DC-link voltages in each phase of the cascaded H-bridge converter separately and the second components allow exchanging the energy between the phases.

Introduction

Multilevel converters have been known for more than thirty years [1] but recently the significant development in research and applications has been observed in this field. One of the most interesting multilevel converters is the cascaded converter due to its modularity and the smallest number of components compared to other topologies. The cascaded H-bridge (CHB) converter (Fig. 1) demands separate DC sources which are usually supplied from a multi-winding transformer in electric drive applications. In STATCOM applications with a CHB converter the DC-link is distributed which enables using an increased number of low voltage energy storages, but causes problems with DC-link voltage unbalance. Many papers are devoted to the DC-link voltage balancing in multilevel converters [2], [3], [4]. This problem can be solved by modifying the modulation strategy [3], specific topology of the converter [2] or using multi-winding transformers [1], [5]. The paper presents the DC-link voltage balancing method applied to the CHB converter without using additional power circuit components, which is based on the same approach as in [3]. In paper [3] the balancing method was applied for the single-phase five-level CHB converter operating as a rectifier where the fundamental component of the AC-side current was in phase with the AC line voltage. Here, the proposed method is implemented in a three-phase converter and does not draw active power from the AC source. The method demands a continuous flow of reactive phase current and is based on the injection of additional output voltage components that exchange active power between H-bridge converters. Active power in a CHB converter can be exchanged between H-bridge converters inside each phase and between the phases; thus two balancing schemes are distinguished – the inphase balancing scheme and interphase balancing scheme. The US patent [6] presents a similar approach but the application of

that balancing method can influence phase currents. The application of the proposed method does not change phase currents if modulating signals do not exceed their limits.
The paper introduces the CHB converter with its modulation strategy based on phase-shifted PWM, then thoroughly presents the inphase and interphase DC-link voltage balancing schemes. These schemes have been experimentally verified by the laboratory model of the power conditioning system (PCS) with a five-level CHB converter. The paper also focuses on the possibility of extending the proposed method into higher level converters, which has been proved by simulation results for the seven-level CHB converter.

Cascade H-Bridge multilevel converter under phase-shifted PWM

CHB converters consist of H-bridge converters that are connected in series in each phase of the converter. In the case of the five-level converter two H-bridge converters are used in each phase as shown in Fig. 1. The AC-side output voltage of the single-phase leg of the converter v_{cA} is the sum of the output voltages of both H-bridge converters $v_{cA} = v_{cA1}+v_{cA2}$.

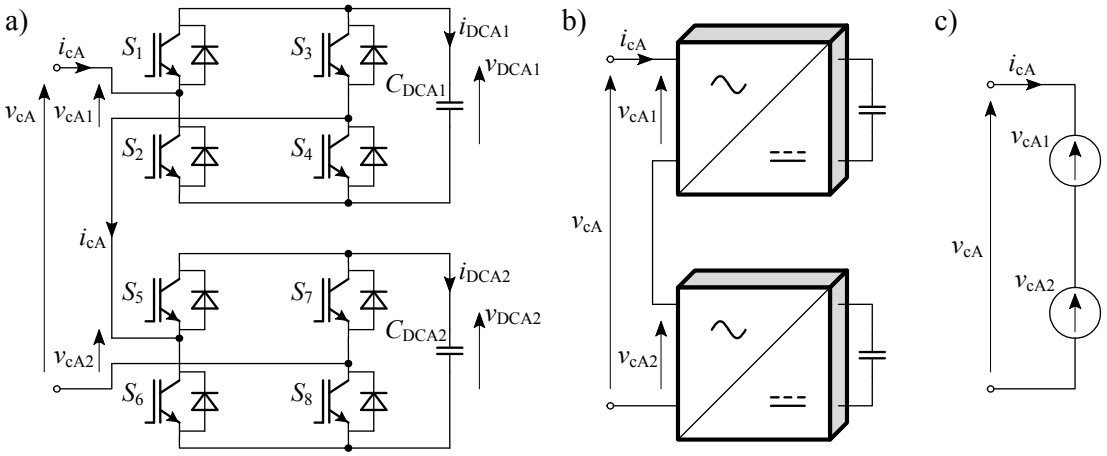

Fig. 1: Single-phase leg of the five-level cascaded H-bridge converter: a) the power part circuit, b) the block diagram, c) simplified circuit

One of the most commonly used pulse width modulation methods for CHB multilevel converters is the phase-shifted pulse width modulation (PSPWM). The PSPWM method for the single-phase leg of the converter is illustrated in Fig. 2. In the PSPWM method the switching signals s_1, s_4, s_5 and s_8 are produced by comparing the modulating signal S_M, which is characterised by the amplitude A_M and frequency f_M, with uniformly phase-shifted triangular carrier signals S_{N1}–S_{N4}, which have the same peak values A_N and the carrier frequency f_N. The carrier frequency determines the switching frequency of transistors, thus $f_S = f_N$. Other switching signals (s_2, s_3, s_6 and s_7) are complementary to signals s_1, s_4, s_5 and s_8 respectively. Similarly to other PWM methods, two modulation indices can be defined for the PSPWM method. They are the amplitude modulation index $m_a = A_M/A_N$ and frequency modulation index $m_f = f_N/f_M$. One can see from Fig. 2 that switching signals affect the output voltages v_{cA1}, v_{cA2} and DC-link currents i_{DCA1}, i_{DCA2}, which can be expressed by (1) and (2) respectively.

$$v_{cA1} = v_{DCA1}\left(s_1 - \overline{s_4}\right),\ v_{cA2} = v_{DCA2}\left(s_5 - \overline{s_8}\right) \tag{1}$$

$$i_{DCA1} = i_{cA}\left(s_1 - \overline{s_4}\right),\ i_{DCA2} = i_{cA}\left(s_5 - \overline{s_8}\right) \tag{2}$$

The effective switching frequency in the H-bridge converter output voltage v_{cAx} is two times higher than the switching frequency f_S (Fig. 2b) [1]. Since the output phase voltage v_{cA} is the sum of voltages v_{cA1} and v_{cA2}, $v_{cA} = v_{cA1}+v_{cA2}$, the effective switching frequency observed in the output voltage of the five-level CHB converter is four times higher than the switching frequency f_S. This means that in each switching period T_S there are four pulses which have the same width and are uniformly distributed. The effective switching frequency increase is one of the most important advantages of the CHB multilevel converter and allows using smaller reactive filters in the AC-side of the converter.

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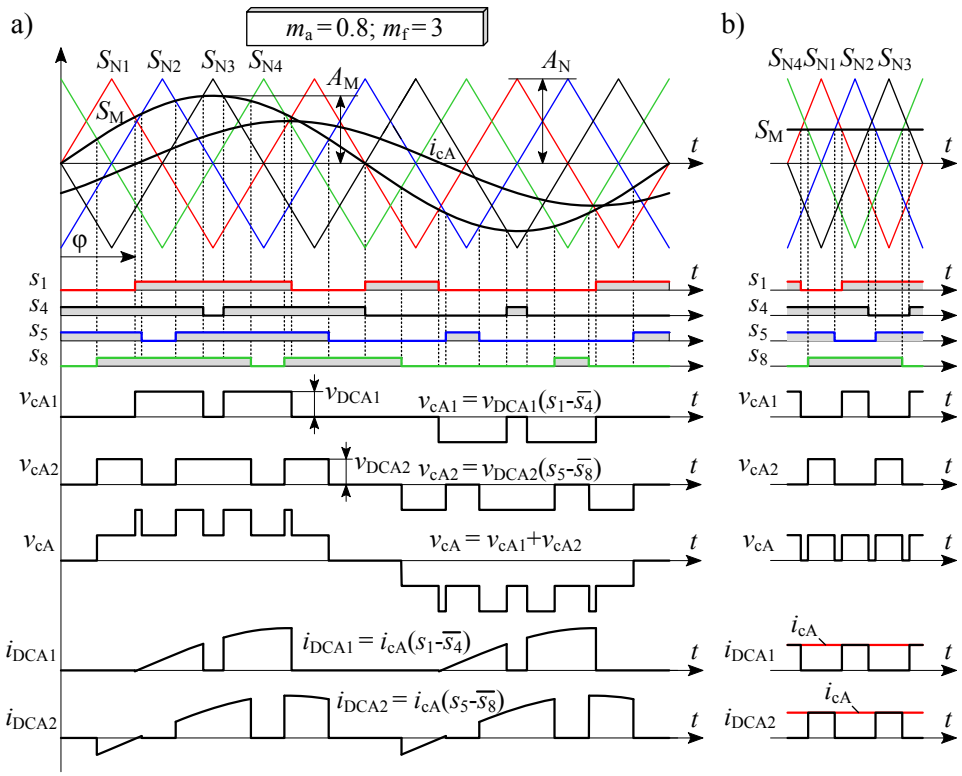

Fig. 2: Phase-shifted PWM (PSPWM) method for the five-level CHB converter: a) the output voltages and DC-link current waveforms ($m_a = 0.8$, $m_f = 3$, $\varphi = 45^o$), b) the waveforms during $T_S = 1/f_S$

When switching signals are averaged over the switching period T_S and an assumption is made that $m_f > 20$, equations (1) and (2) can be rewritten into (3) and (4).

$$v^*_{cA1}\Big|_{T_S} = v_{DCA1} S_M,\ v^*_{cA2}\Big|_{T_S} = v_{DCA2} S_M \tag{3}$$

$$i^*_{DCA1}\Big|_{T_S} = i_{cA} S_M,\quad i^*_{DCA2}\Big|_{T_S} = i_{cA} S_M \tag{4}$$

From equation (4) it can be seen that the averaged DC-link currents are the same, which makes the DC-link voltages balanced. This is valid only for an ideal CHB converter made of the same semiconductor devices, capacitors and with a PWM modulator which generates switching signals that are uniformly distributed in the switching period with exactly the same duty cycles. The aforementioned conditions in CHB multilevel converters are hard to be met in practice and for this reason the DC-link voltage balancing method is of great importance for the proper operation of a converter. The proposed DC-link voltage balancing method is based on the insertion of additional components into the modulating signals S_M of each H-bridge converter. Thus the usage of the same modulating signal S_M for each H-bridge converter existing in a particular phase is no longer valid. It is assumed that all of the modulating signals are updated only one time per switching period T_S.

DC-link voltage balancing method

The main task of the DC-link voltage balancing control method for the CHB converter is to keep DC-link voltages at a required level without affecting the output voltage of the AC-DC converter v_c and phase currents i_c. Two balancing schemes are presented in this paper. Both schemes are based on generating additional voltage components across the outputs of H-bridge converters, which together with the output current i_c causes an active power flow between the H-bridge converters. It is important that these additional voltage components should have the same frequency as the phase current i_c (equal to the fundamental frequency of 50 Hz). The first scheme, named the inphase DC-link voltage balancing scheme, exchanges the balancing active power between the H-bridge converters inside a

particular phase. The second, the interphase DC-link voltage balancing scheme, allows active power exchange between the CHB converter phases. Both balancing schemes are explained in detail in the following subparagraphs. An analysis has been carried out assuming that the sum of DC-link voltages (in three phases) is equal to the required value and currents in the PCS are symmetric and sinusoidal. When the sum of DC-link voltages (in three phases) differs from the required value, this sum is stabilized by using the DC-link voltage controller (REG1 in Fig. 8).

Inphase DC-link voltage balancing

This balancing scheme for the (2*n*-1)-level CHB converter is based on the insertion of additional voltage balancing components v_{bYx} in the output voltages of each of *n* H-bridge converters (where x = 1, ..., *n*) in such a manner that the sum of these additional components in phase Y (Y = A, B or C) always equals zero – Fig. 3. These voltage components are in phase or in antiphase with the current i_{cY}. Each phase of the CHB converter is treated separately. The phase DC-link voltage balancing components $\underline{V}_{bYx}$ in a vector form are expressed by the equation (5).

$$\underline{V}_{bYx} = -k_{b1}\left(v_{DCYx} - \frac{1}{n}\left(\sum_{k=1}^{n} v_{DCYk} \right) \right) \hat{\underline{I}}_{cY} \tag{5}$$

where: $\hat{\underline{I}}_{cY} = \dfrac{\underline{I}_{cY}}{\|\underline{I}_{cY}\|}$ is the unit vector of the phase current i_{cY} and k_{b1} is the proportional coefficient.

The coefficient k_{b1}, together with the amplitude of the phase current I_{cYm}, determines the balancing process time. To keep the constant balancing process time the coefficient k_{b1} has to be dependent on I_{cYm}. During the experiments the value of $k_{b1} \approx 1$ V/V gave satisfactory results. One can see from (5) that when the voltage of the *x*-th H-bridge converter v_{DCYx} is higher than the average value of DC-link voltages in phase Y, the balancing component $\underline{V}_{bYx}$ is in antiphase with the current $\underline{I}_{cY}$, what means that active power should be taken from the DC-link of such a H-bridge converter. When the voltage v_{DCYx} is lower than the average value of DC-link voltages, the active power is delivered to the DC-link capacitor. The principle of the inphase DC-link voltage balancing is depicted in Fig. 3.

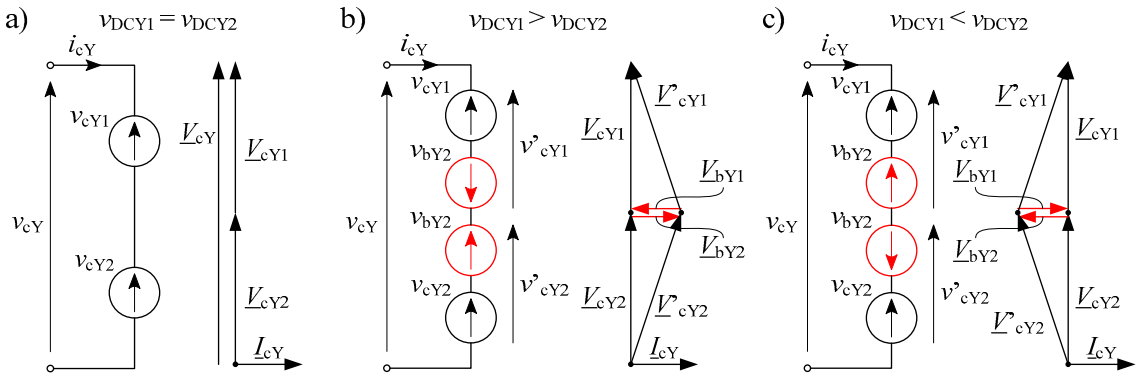

Fig. 3: Inhase DC-link voltage balancing operating in phase Y for the five-level CHB converter

It can be proved by (6) that the sum of vectors $\underline{V}_{bYx}$ in each phase Y is equal to zero.

$$\sum_{k=1}^{n} \underline{V}_{bYk} = -k_{b1} \sum_{k=1}^{n} \left(v_{DCYk} - \frac{1}{n}\left(\sum_{k=1}^{n} v_{DCYk} \right) \right) \hat{\underline{I}}_{cY} = -k_{b1} \left(\sum_{k=1}^{n} v_{DCYk} - \sum_{k=1}^{n} v_{DCYk} \right) \hat{\underline{I}}_{cY} = 0 \tag{6}$$

The inphase DC-link voltage balancing is also illustrated with waveforms in Fig. 4. The case for balanced voltages $S_{MA1} = S_{MA2}$ is given in Fig. 4a. The phase DC-link voltage balancing components change modulating signals S_{MYx} and the width of corresponding pulses in output voltages (Fig. 4b). The experimental results for the five-level CHB converter during the start-up of the inphase DC-link voltage balancing are presented in Fig. 4c. The oscilloscope traces show the phase current i_{cA} during 1 ms. One can see that the balancing scheme does not change the current low frequency component. The inphase DC-link voltage balancing in the output voltage changes only the distribution of pulses

 ISBN: 9789075815153

with the same width. If the balancing components cause an increase of modulating signals over their limits ($m_a = 1$ or $m_a = 1.15$ for third harmonic injection), the operation instabilities of the CHB converter can occur – they may be observed for example in grid currents. This implicates the need of the coefficient k_{b1} limitation.

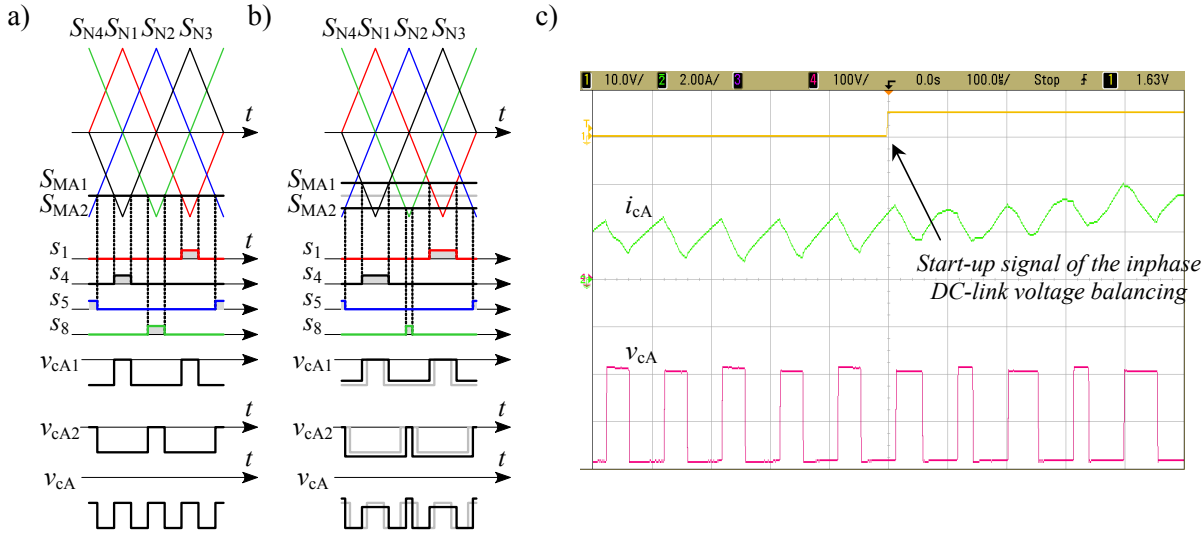

Fig. 4: Principle of the inphase DC-link voltage balancing: a) operation in case of $S_{MA1} = S_{MA2}$ ($v_{DCA1} = v_{DCA2}$), b) operation in case of $S_{MA1} > S_{MA2}$ ($v_{DCA1} < v_{DCA2}$), c) experimental results for the CHB converter connected to the grid ($f_S = 2550$ Hz, time scale: 100 µs/div, output voltage: 100 V/div and current: 2 A/div)

The application of the phase DC-link voltage balancing ensures the same DC-link voltages in each phase separately. When the sums of the DC-link voltages in the phases differ from each other, these sums can be balanced by using the interphase DC-link voltage balancing scheme.

Interphase DC-link voltage balancing

This DC-link voltage balancing scheme is based on AC common-mode (zero sequence) voltage components, which with the phase currents can transfer active power between the phases without any impact on the phase and line-to-line voltages of the CHB converter. The use of this scheme is limited to three-phase three-wire systems where the common-mode component does not affect phase currents. To provide an active power flow between DC-link capacitors, the common-mode components used in this scheme should have the same frequency as the phase currents. It is assumed that the sum of all $3n$ DC-link voltages of $(2n\text{-}1)$-level CHB converter is equal to the required value $3n\ V_{DCreq}$.
In Fig. 5a the vector diagram of the three-phase CHB converter output voltages $\underline{V}_{cA}$, $\underline{V}_{cB}$, $\underline{V}_{cC}$ and their phase currents $\underline{I}_{cA}$, $\underline{I}_{cB}$, $\underline{I}_{cC}$ is presented. It is based on the assumption that phase current vectors are perpendicular to output voltages having an inductive phase angle. The common-mode voltage component V_{b2} is added to each CHB converter output voltage, as shown in Fig. 5b, and interacts with phase currents causing an active and reactive power flow between the converter phases. Only the active power flow can be utilized to balance the DC-link voltages of a CHB converter. The complex plane presented in Fig. 5a is divided into six sections **I-VI** where active powers have different signs. For example, if the vector of the balancing voltage component $\underline{V}_{b2}$ is in section **I**, the active power in phase A and C is positive $P_A > 0$, $P_C > 0$ and in phase B is negative $P_B < 0$. It means that the DC-link capacitors in phase A and C are charged with the energy taken from the DC-link capacitors in phase B. The common-mode balancing vector $\underline{V}_{b2}$ is made up of three balancing vectors that are collinear with phase currents respectively, the magnitudes of which are proportional to the differences between the sums of DC-link voltages in each phase and the average value of DC-link voltages V_{DCABC} – Eq. (7).

$$\underline{V}_{b2} = -k_{b2}\left(\left(\sum_{k=1}^{n} v_{DCAk} - V_{DCABC}\right)\hat{\underline{I}}_{cA} + \left(\sum_{k=1}^{n} v_{DCBk} - V_{DCABC}\right)\hat{\underline{I}}_{cB} + \left(\sum_{k=1}^{n} v_{DCCk} - V_{DCABC}\right)\hat{\underline{I}}_{cC}\right) \qquad (7)$$

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where $V_{\mathrm{DCABC}} = \frac{1}{3}\sum_{\mathrm{Y=A,B,C}}\sum_{k=1}^{n} v_{\mathrm{DCYk}}$ is the average value of the sum of DC-link voltages in each phase.

This approach ensures the minimization of active power needed for interphase DC-link voltage balancing.

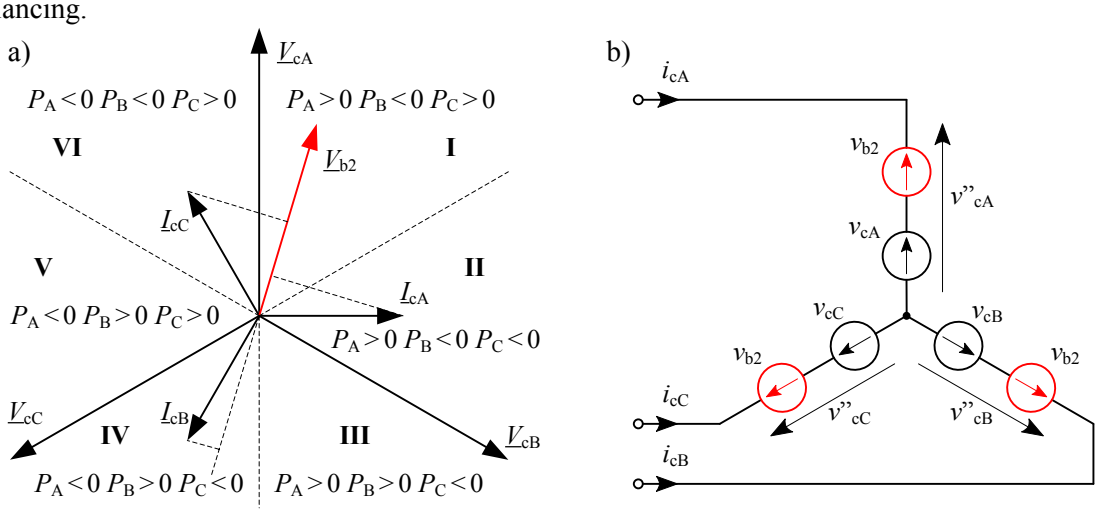

Fig. 5:Interphase DC-link voltage balancing: a) the vector diagram presenting the interaction of the common-mode balancing vector $\underline{V}_{\mathrm{b2}}$ on active powers P_{A}, P_{B} and P_{C}, b) corresponding circuit

In Fig. 6 it can be seen that the interphase DC-link voltage balancing changes the output voltage and its average (over period T_{S}) value. It does not influence phase currents because the same changes of output voltages exist in other phases of the CHB converter. The delay t_{delay} between the start-up signal and the change of the pulse width presented in Fig. 6c comes from the delay of double buffered registers in microcontroller PWM modules. One can see that after starting up of the balancing, the output voltage v_{cA} rapidly changes its average value by about 60 V. If such a change existed in the inductor voltage, it would cause a rapid change of the current derivative. One can see that this rapid change is not observed, which proves the correctness of the interphase DC-link balancing.

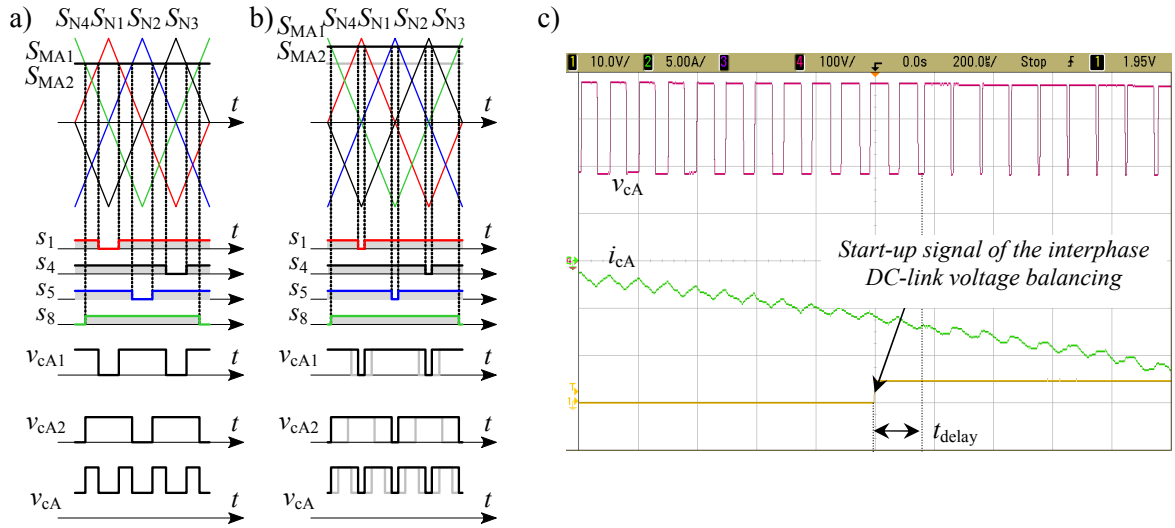

Fig. 6: Principle of the interphase DC-link voltage balancing: a) operation without balancing, b) operation with both modulating signals $S_{\mathrm{MA1}} = S_{\mathrm{MA2}}$ changed, c) experimental results for the CHB converter connected to the grid (f_{S} = 2550 Hz, time scale: 200 µs/div)

Limitations of DC-link voltage balancing method

The main limitation of the proposed DC-link voltage balancing method is overmodulation that occurs when modulating signals S_{M} are higher than the carrier signals S_{N}. The largest output voltage v_{c} in the PCS is produced when inductive reactive power is delivered to the grid. The voltage v_{L}, across the

line inductors L_{AC} is the difference of the grid voltage v_s and the converter voltage v_c. This voltage depends on the demanded current generated by the PCS and the reactance ωL_{AC}. In the case of voltage harmonics at the grid, the PCS must also generate the same voltage harmonics which may increase the modulating signals. Moreover, the PCS can also be capable of generating current harmonics (for load current harmonic elimination), which is also connected with additional components in the modulating signals. To avoid overmodulation, all these modulating signal components should be taken into consideration and finally the coefficients k_{b1}, k_{b2} in the proposed balancing method must be limited.

Laboratory prototype of power conditioning system

The laboratory prototype of the power conditioning system with a five-level CHB converter and supercapacitors is shown in Fig. 7 [7]. It has a nominal power of 10 kVA and is supplied from the three-phase, three-wire 400 V, 50 Hz grid through three 4 mH inductors L_{AC}. Each of the six DC-link circuits has a capacitance of C_{DC} = 4.4 mF with the required DC-link voltage V_{DCreq} = 190 V. The maximum energy of supercapacitors is 300 kJ (6x7,25 F, 120 V) and they are connected to DC-link capacitors through DC-DC converters. Although the operation of supercapacitors can be useful for the DC-link voltage balancing, during the steady state they are switched off and for this reason have been omitted in this paper. The switching frequency is f_S = 2.55 kHz [8].

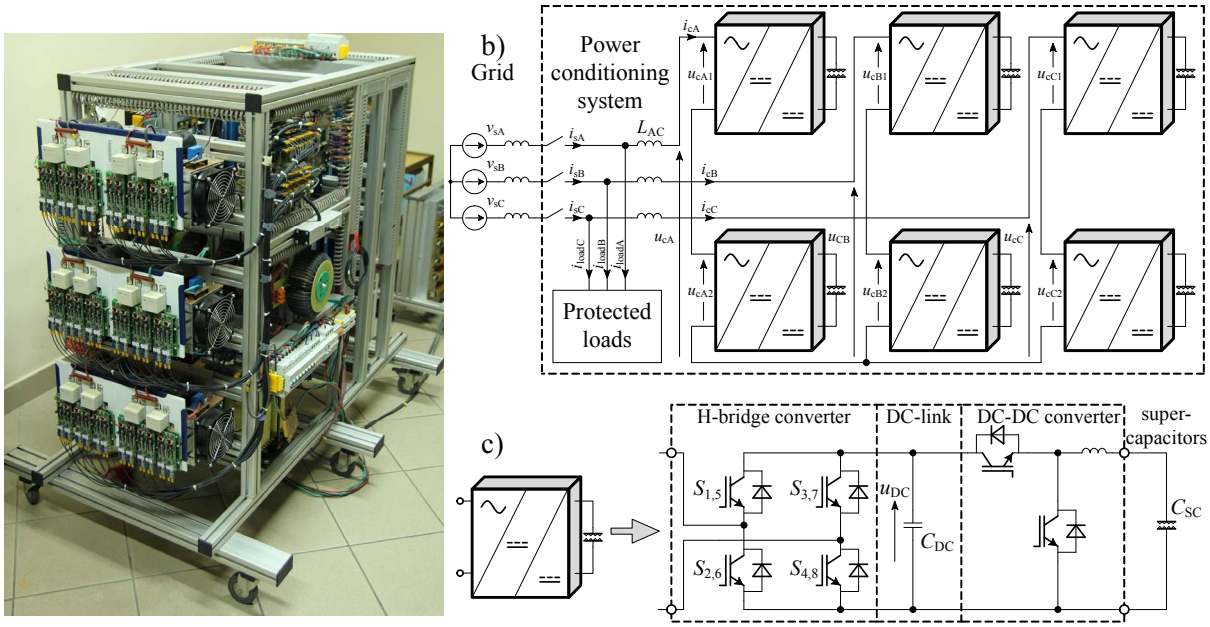

Fig. 7: The laboratory prototype of the power conditioning system with a five-level CHB converter

The control system of the laboratory prototype (Fig. 8) is similar to control systems of converters with a single DC-link circuit. It is divided into two parts, first for the AC-DC (CHB) converter and the second part is the controller of six DC-DC converters. The controller of the AC-DC converter is responsible for controlling AC side currents of the PCS i_c or voltages across the protected load v_{load}. The controller of the DC-DC converters controls the energy delivered to or taken from the supercapacitors. The paper focuses on the DC-link voltage balancing method, so the issues related to the controller of the AC-DC converter have been maximally simplified in this part. As was mentioned, the controller of multilevel CHB converter operates similarly to the two-level converter controller, with a certain modification, namely the DC-link voltage controller (REG1) controls the average value of all six DC-link voltages ½ V_{DCABC}. The DC-link voltage controller controls the active (d-axis) current i_{DCd} in such a manner that the PCS eliminates all non-active currents from the load current (i_{loadq} and i_{loadd}-i_{DCd}). This is sufficient to produce sinusoidal grid currents that are in phase with grid voltages. The inner current control loop generates CHB converter voltage signals ensuring the required AC-side phase currents i_c. Taking into account the actual six DC-link voltages v_{DCYx}, the modulating signals S_{MYx} are computed and modified by additional signals generated in DC-link voltage balancing blocks according to equations (5) and (7). The control system was implemented in the digital signal microcontroller TMS320F2808 [9].

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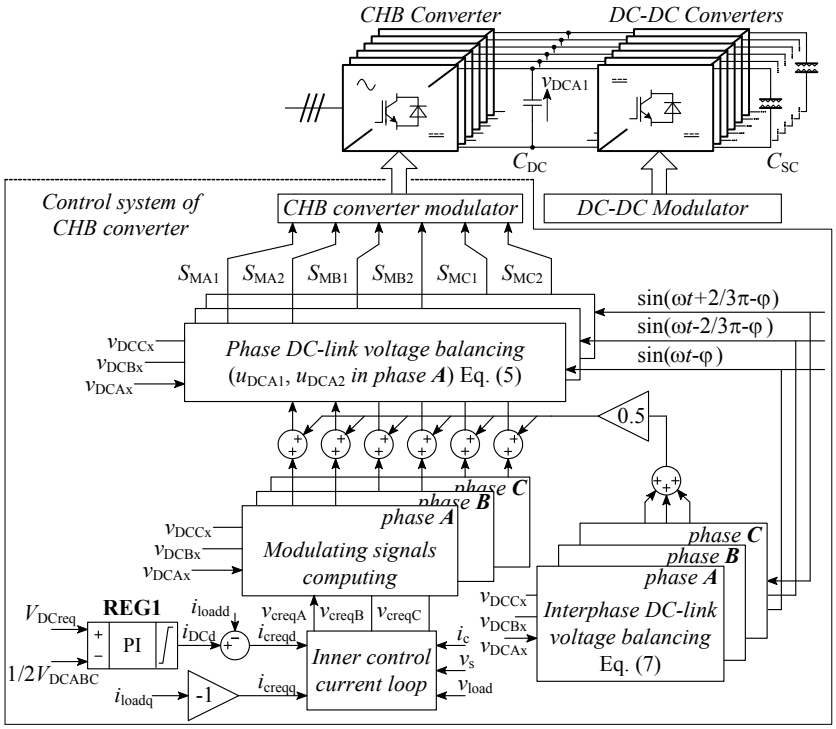

Fig. 8: Controller of the power conditioning system with a five-level cascaded H-bridge converter

Experimental results

The operation of the proposed DC-link voltage balancing method implemented in the laboratory prototype of the PCS with a five-level CHB converter is illustrated in Fig. 9.

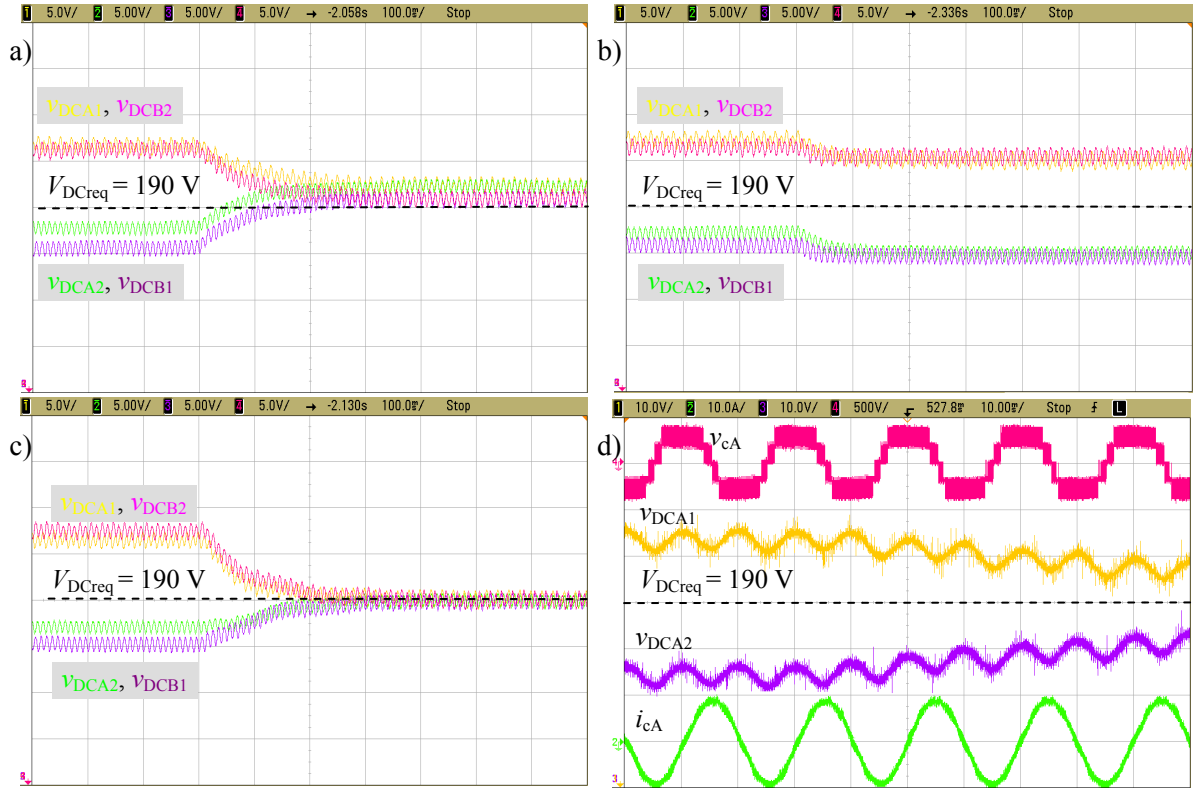

Fig. 9: Operation of the DC-link voltage balancing method (100 ms/div): a) the inphase balancing, b) the interphase balancing, c) both inphase and interphase balancing, d) CHB voltage and current with phase A DC-link voltages after start up of the proposed balancing method (10 ms/div)

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Fig. 9 presents four of the six DC-link voltages – when the DC-link voltage balancing method was tested with an inphase (Fig. 9a), interphase (Fig. 9b) and both schemes together (Fig. 9c). In all experiments the phase current amplitude was equal to 9 A. One can see from these oscilloscope traces that DC-link voltages in each phase tend to be equal (Fig. 9a), the average values of DC-link voltages in each phase tend towards the required DC-link voltage V_{DCreq} (Fig. 9b) and all DC-link voltages tend to V_{DCreq} (Fig. 9c). The lack of the influence of the proposed DC-link voltage balancing method on phase current i_{cA} (Fig. 9d) proves it correctness. All experiments were performed for proportional coefficients $k_{b1} = k_{b2} = 0.5$. During the tests the balancing ability was successfully examined for different current amplitudes and for inductive and capacitive phase angles.

Simulation results for the DC-link voltage balancing method

The proposed DC-link voltage balancing method has been examined for higher than five-level CHB converters by modeling and simulating the seven-level CHB converter in Matlab-Simulink. It has three H-bridge converters in each phase (Fig. 10b) and is connected to the grid (400 V line-to-line voltage) – Fig. 10a. DC-link circuit parameters are as follows $C_{DC} = 10$ mF, $V_{DCreq} = 130$ V and other parameters are the same as in the laboratory prototype presented in previous paragraphs.

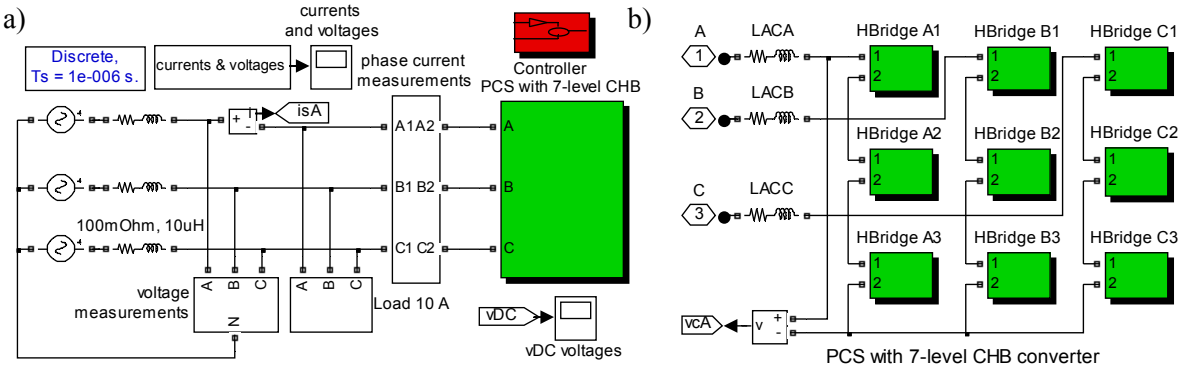

Fig. 10: Matlab-Simulink simulation model of the PCS with a seven-level CHB converter: a) the main circuit, b) the seven-level CHB converter

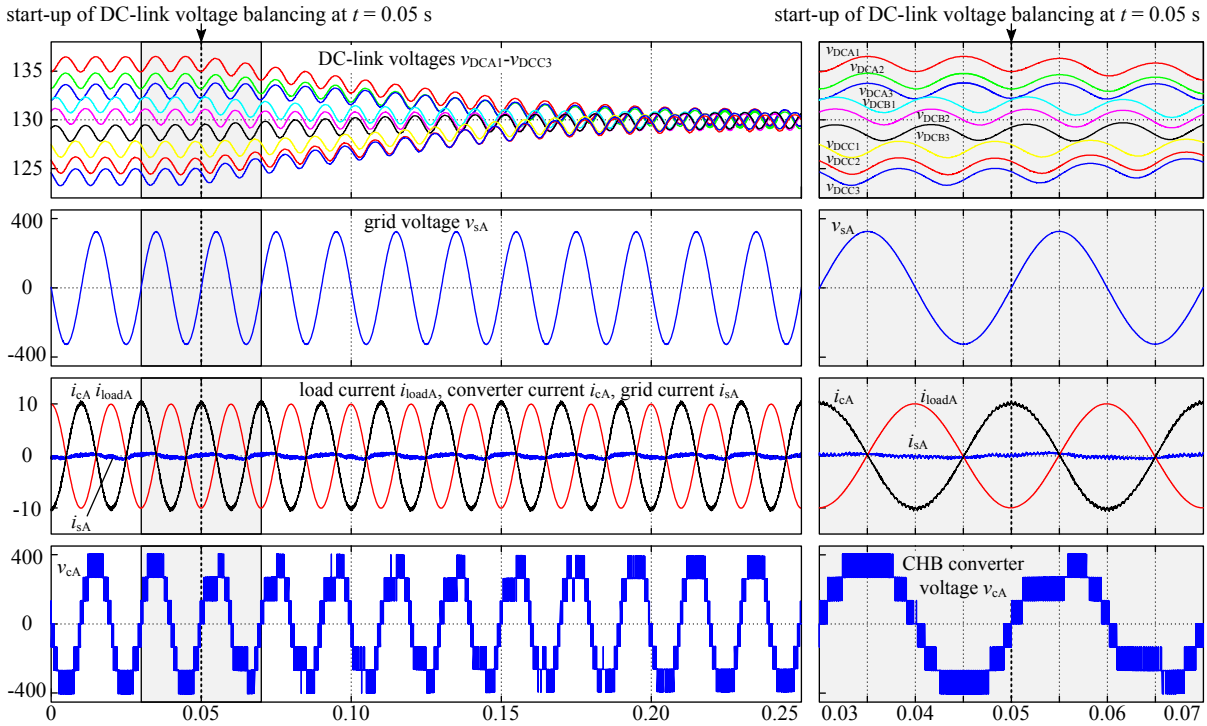

Fig. 11: Simulation waveforms of the seven-level CHB converter operating in the PCS. From top: all nine DC-link voltages: $v_{DCA1} - v_{DCC3}$ ($V_{DCreq} = 130$ V), the grid voltage v_{sA}, the grid current i_{sA}, the load current i_{loadA} and the CHB converter current i_{cA}, the CHB output voltage v_{cA}

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Fig. 11 shows that the CHB converter operates properly under the operation of the DC-link voltage balancing method. At the beginning of the presented simulation all the DC-link voltages are unbalanced. After turning on both DC-link voltage balancing schemes all DC-link voltages tend towards the required value V_{DCreq} = 130 V. It changes the CHB converter voltages in such a manner that there is no influence of the voltage balancing method on the operation of the whole PCS (no disturbances in the currents i_c are observed). Obviously, this is true if the modulating signals in all CHB converters do not exceed the limitations. For this reason the proportional coefficients k_{b1}, k_{b2} should be relatively low. In the grid current, during the simulation, the small active component exists in the phase current, which comes from the power losses in the CHB converter.

Conclusion

In the paper the DC-link voltage balancing method for the cascaded H-bridge multilevel converter is presented. Their principal use is in STATCOM applications where there is no large unbalance in converter AC-side output currents. The presented method does not need to use any additional power circuits for balancing voltages; it only requires the application of the control system of the PCS with a CHB converter. For proper operation the DC-link voltage balancing method requires a continuous flow of phase currents, which can transfer the balancing energies between DC-link circuits. This problem can be avoided in the STATCOM application by ensuring a low threshold of phase currents. The drawback of the proposed method is the need to use voltage measurements of all DC-link capacitors, which increases the complexity of the system. In multilevel converters these measurements are normally performed for safety reason; therefore, these measurements can also be utilized for voltage balancing.
The proposed method has been experimentally verified by using the laboratory prototype of the power conditioning system with a five-level cascaded H-bridge converter and supercapacitor energy storage. It was also examined by the simulation of the seven-level CHB converter. Both experimental and simulation results prove the proper operation of the DC-link voltage balancing method.

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