Multilevel Converter for Power Conditioning System with SMES

Abstract: Multilevel converters have emerged recently as power electronic converters for high voltage and power applications. The analysis of converter topologies and control strategies for multilevel converters enabling two-quadrant operation in power conditioning system PCS with superconducting magnetic energy storage SMES is given in the paper. Diode-clamped, capacitor-clamped and cascaded converters are explored and compared. Three-level diode-clamped converter with space vector pulse width modulation has been selected.

Stresszczenie. Falowniki wielopoziomowe pojawiły się stosunkowo niedawno jako przekształtniki do zastosowań przy średnich napięciach oraz wysokiej mocy. Artykuł zawiera analizę kilku topologii przekształtnika wielopoziomowego jak i sposobu jego sterowania. Analiza jest prowadzona ze względu na przydatność przekształtnika wielopoziomowego w kondycjonerze mocy z magazynowaniem energii w cewce z nadprzewodnika. Artykuł zawiera porównanie przekształtników wielopoziomowych: z diodami poziomującymi, z kondensatorami poziomującymi oraz falownika kaskadowego.

Keywords: multilevel converters, voltage balancing, multilevel vector PWM, power converters

Słowa kluczowe: przekształtniki wielopoziomowe, stabilizacja napięć w obwodzie pośrednim, wielopoziomowa metoda modulacji, szerokość impulsów, przekształtniki energoelektroniczne.

Introduction

Multilevel converters (power electronic converters) in application to Power Conditioning Systems (PCS) are the subject of the paper.

The selection of the best multilevel converter topology (together with control strategy) that could operate in the PCS is the aim of the work.

Multilevel converters can be roughly described using Fig. 1 where the schematic diagram and a selected waveform of the output voltage are given.

![Figure 1: Multilevel converter with one phase leg.](image)

Fig. 1. Multilevel converter. (a) Schematic diagram of one phase leg. (b) Output voltage waveform of n-level converter.

Number of voltage levels \( n \) is the attribute of multilevel converter. It is defined as the number of levels in output voltage \( u_{\text{AC}} \) measured between output terminal \( A \) and the neutral point 0 or negative terminal of DC link [3]. It is explained in Fig. 7 given for \( n = 5 \).

Assuming that there is no DC component in output voltage \( u_{\text{AC}} \) and \( u_{\text{L}} \) is symmetric the converter \( C \) has to be supplied by \( n-1 \) voltage sources \( U_{P1}, U_{P2}, \ldots, U_{P(n-1)/2}, U_{N1}, U_{N2}, \ldots, U_{N(n-1)/2} \), that are different from each other.

Equality of positive and negative voltages \( U_{P1} = U_{N1}, \ldots, U_{P(n-1)/2} = U_{N(n-1)/2} \) is one of two conditions that should be fulfilled in order to get symmetrical output voltage waveform. The second condition is symmetry in the switching times.

Power Conditioning System (PCS) is depicted in Fig. 2. Assuming the symmetry and the lack of DC component in the output voltage \( u_{\text{AC}} \) the converter \( C \) has to be supplied by \( n-1 \) voltage sources. The sources are different from each other. PCS consists of two converters (AC-DC and DC-DC) and energy storage (in this case superconducting magnetic energy storage (SMES)). In normal state of mains the energy is delivered from mains to (protected) load (e.g. paper machines) while SMES (in other words inductor \( L_{\text{SMES}} \)) stores certain amount of energy. In case of the faults in the mains the circuit breaker is off and the energy is immediately drawn out from the SMES being delivered to the load for the certain time.

PCS with SMES is highly dynamic system that starts the transfer energy from the SMES to the protected load in time of about 5 ms. The stored energy is enough till the conventional source of energy is turn on (fuel cells, diesel generator). The energy flow between mains and SMES and between SMES and the load is maintained by converters.

It is necessary to add that the faults means voltage sags, swells, and power interruptions. Instead of SMES super capacitor could be used.

![Figure 2: Power conditioning system PCS with multilevel converters](image)
Apart from delivering energy to the load PCS can operate like reactive power compensator and active filter of higher harmonic content in currents taken from mains.

Contemporary PCSs need to be built for high rated power and high rated energy. High power can be achieved at high rated voltage.

The relevant rated voltage can be obtained by application of two-level converters with transistors/GTOs connected in series or/and by applications of transformers. Instead of two-level converters it is possible to use multilevel converters. Besides high rated voltage the advantage of it is much better shape of its AC current in comparison with AC current in two-level converters. The AC-DC converter in this case is voltage source converter.

Having such precisely described topic one can state that the thorough examination of (power electronic) multilevel converters is needed. The control of the whole PCS is outside the scope of the paper.

It is necessary to stress that study of literature of the subject revealed the lack of papers reporting the results of such research works as is presented in this paper.

The following assumptions have been made for the analysis of AC-DC converter:

1) Multilevel converter should operate as: i) reactive power compensator; ii) active power filter and iii) high dynamics UPS (with SMES); iv) should be immune against voltage sags, swells, and power interruptions.

2) Converter should maintain balanced voltages across DC link capacitors, it means every voltage level should be stabilized at needed level.

3) The power part of the converter should be transformerless.

The work is a theoretical one basing on analysis that is carried out using Matlab-Simulink.

The structure of the paper is as follows. It encompasses:

i) classification of multilevel converter topologies, ii) diode-clamped converter, iii) capacitor-clamped converter, iv) cascaded multilevel converter, v) comments on power part of multilevel converters vi) classification of control strategies, vii) selective harmonic elimination, viii) space vector control, ix) sinusoidal pulse width modulation, x) comments on modulation strategies and xi) conclusions.

**Classification of multilevel converter topologies**

The multilevel concept comes from ideas of step approximation of sinusoid that was patented by the MIT researcher [1], [2]. As was mentioned above multilevel AC-DC converters have to be used when high rated voltage is needed as well as good shape of AC current of the converter is demanded. In multilevel converter single device has to withstand only small part of the DC link voltage $U_{DC}$. Voltage across the switch depends on number of output voltage levels $n$ and is equal to $\frac{U_{DC}}{n-1}$, cf. Fig. 8 where $n = 5$. Although it is possible to have any number of levels it is usually limited to $n = 10$ [3], [4], because of the complexity of its control.

Apart from operation at high voltage level multilevel converters assure small dv/dt and low voltage THD. It results in smoother AC currents. Smaller dv/dt results in low EMI problems.

For three-phase converters number of levels in line-to-line voltage and in phase voltage differs from number of levels of output voltage. For three-phase symmetrical converter the number of levels in line-to-line voltage is $(2n-1)$ but phase voltage has more levels where the maximum number of levels is $(4n-3)$. In this paper essentially only five-level converters for PCS (Fig. 2) are taken into consideration, with 9 levels in line-to-line voltage and 17 levels in phase voltage. Number of voltage levels in phase voltage is a function of modulation index.

There are three basic types of converters (topologies) existing in the class of multilevel converters. They are: diode-clamped converters – DCC (derived from neutral-point clamped NPC inverter [5]), capacitor-clamped converter- CCC (flying capacitors or multicell converter) [3], [4], [11], and cascaded multicell converter – CMC (H-bridge) [3], [4] and [7]. All the topologies are compared in this paper in terms of usefulness in PCS with SMES. Each topology can operate as rectifier or inverter resulting in different energy flow direction. All of them have the same number of switches but use different number of capacitors and diodes and can be controlled under different control strategies. The control strategies are described in the second part of this paper.
Diode-clamped converter (DCC)

The first mention of diode-clamped converter DCC can be found in paper [5] where authors proposed neutral point clamped (NPC) inverter that produces three-level output voltage Fig. 3. Multilevel diode-clamped converters based on NPC structure instead of two pairs of switches in every phase leg of three-level converter have \( n-1 \) pairs of switches cf. Fig. 4 and Fig. 5. Switches \( S_1-S_1', S_2-S_2', \ldots \) are complementary.

Turned on transistor caused that the voltage from related capacitor is connected to the output. Diodes have to block capacitors when greater voltage is at output terminal. This means that voltage across every diode is equal to \( U_{DC}/(n-1) \).

Because there are \( n-1 \) complementary switch pairs in every phase leg they can be switched on/off in \((n-1)^2\) manners. Only \( n \) switching states allow generating output voltage by connecting AC load to DC link capacitors. For \( n = 5 \) these states are depicted in Fig. 6 with indication of corresponding current paths in one phase leg for both current direction flows.

![Fig.6. Equivalent circuits for five states of upper switches of one phase leg of diode-clamped converter; \( n = 5 \)](image)

\[ u_{\text{in}} = \frac{U_{DC}}{2} \]
\[ u_{\text{in}} = \frac{U_{DC}}{4} \]
\[ u_{\text{in}} = 0 \]
\[ u_{\text{in}} = -\frac{U_{DC}}{4} \]
\[ u_{\text{in}} = -\frac{U_{DC}}{2} \]

\[ \text{Switch states: } 1111 \quad 0111 \quad 0011 \quad 0001 \quad 0000 \]

The behavior of voltage unbalancing can be explained using Fig. 7 where waveforms of capacitor voltages are given. The converter directly connected to the DC link, with AC resistive-inductive load, draws currents from certain capacitors that cause capacitor voltage unbalance. In other words the capacitor voltages are not balanced when AC load draws from converter real power. It can be observed in Fig. 7 where waveforms of capacitor voltages are given. The behavior of voltage unbalancing can be explained using Fig. 6 where current paths are presented.

Assuming that the AC load is pure resistive capacitor voltages change their value in states 2 and 9, that is when output voltage is equal to \( \frac{1}{4} U_{DC} \) or \( -\frac{1}{4} U_{DC} \). For state 2 \((u_{\text{in}} = \frac{U_{DC}}{4})\) current flowing through capacitor \( C_4 \) is greater than current of \( C_1 \) and \( C_2 \) because serial connection of three capacitor give smaller capacitance. All four capacitors are connected to the DC link voltage \( U_{DC} \), thus any increase in voltage at one capacitor is connected with the decrease in voltage across the other capacitors. If current of \( C_4 \) is greater it means that voltage across that capacitor is increasing more than across other capacitors, \( C_1 \), \( C_2 \), \( C_3 \). In states 3 or 8 \((u_{\text{in}} = 0)\) currents of \( C_4 \), \( C_1 \) are equal to the currents of \( C_2 \), \( C_3 \) and their values are zero. For state 9 \((u_{\text{in}} = -\frac{1}{4} U_{DC})\), symmetrical in relation to state 2, current changes its direction and flows to the converter leg and then it spreads out through capacitors. In this case the greater current flows through \( C_1 \) increasing its voltage. That is why voltages across \( C_1 \) and \( C_2 \) increase and voltages across \( C_3 \), \( C_4 \) decrease at every cycle. One can observe that sum of that capacitor voltages is equal to \( U_{DC} \).

In Fig. 8 waveforms of output voltage are given for unbalanced capacitor voltages (the same conditions like in Fig. 7). One can observe a decrease in medium level voltages.

The same mechanism of unbalancing capacitor voltages is in three-phase converter. It can be observed and analyzed assuming that the voltage of common point of three-phase load (wye connection) has approximately the same potential as neutral point 0.

Different situation takes place for pure reactive power drawn from inverter AC output (reactive power compensator). Here the current is always shifted with respect to output voltage by \( \pm \pi/2 \). Output voltage of every converter topology with any controller is even-symmetrical with regard to \( \pi/2 \) and odd-symmetrical in relation to 0 and \( \pi \). In this case reactive current flows from/to converter causing that average (over the period) current of each capacitor is equal to 0 - Fig. 9 (where \( i_{\text{A}} \) is averaged or fundamental component). For example in state 2 that lasts the same time as state 7 current is positive and capacitor \( C_4 \) is charged but in state 7 current has the same value but is negative and capacitor \( C_4 \) is discharged – average value of capacitor current is 0.

![Fig.7. Capacitor voltages for three-phase diode-clamped converter with AC resistive-inductive load under PWM control; \( n = 5 \) (simulation for: \( R = 10 \, \Omega, \, L = 100 \, mH, \, C = 1 \, mF, \, f_0 = 50 \, Hz, \, U_{DC} = 200 \, V \))](image)

![Fig.8. Unbalanced output voltage of five-level diode-clamped converter; \( n = 5 \), the same conditions like in Fig. 7 (simulation)](image)

![Fig.9. One phase leg of diode-clamped converter: output voltage and pure output reactive current with switching states (Fig.8); \( n = 5 \)](image)
In case the converter operates as rectifier converting AC real power into DC power the unbalance of capacitor voltages is different in comparison with that given in Fig. 7. $u_{C1}, u_{C3}$ are decreasing while $u_{C2}, u_{C4}$ are increasing.

Therefore it is obvious that five-level diode-clamped converter itself cannot cope with real power conversion because unbalancing of capacitor voltages occurs. The three-level DCC is the only converter, which allows balancing capacitor voltages for AC real power. It can be obtained by application the control strategy basing on redundant converter vectors [13].

There is no control strategy that can maintain balancing capacitor voltages for AC real power when the number of voltage levels is higher than three. It means there is no control strategy that meet assumed demands.

Beside the three-level balanced solution there are two other solutions applicable to the converters of higher number of levels allowing to keep capacitor voltages balanced.

First solution is based on the back-to-back connection of two multilevel converters (necessarily with the same number of levels). Back-to-back connection allows keeping the voltage at each capacitor close to $U_{DC,n+1}$ by using one converter to generate output voltage and second converter to balance capacitor voltages [14]. Although PCS is composed of two converters and it seems that the solution [14] can be applied in this case the details of PCS reveals difficulty. They come from specific features of SMES coil that has to be kept short-circuited after being loaded till the time its energy is needed by the load. Actually it is impossible to use SMES energy for balancing capacitor voltages. It means that back-to-back connection is not the candidate for PCS application when $n > 3$.

Balancing of capacitor voltages can also be achieved by application of multiple winding transformers with rectifiers, each of which supplies its own capacitor. But this solution is bulky in comparison with transformerless one. Therefore this solution is also not the one that can be applied in PCS.

Second multilevel topology is capacitor-clamped converter, CCC also known as flying capacitor or multicell converter [11]. Its structure is presented in Fig. 10 – one phase leg and Fig. 11 – three-phase converter. Voltage across every clamping capacitor has the same value equal to $U_{DC,n+1}$. In case of series connection of clamping capacitors voltage across clamping capacitor branch is a multiple of $U_{DC,n+1}$ (e.g. voltage across $C_3$ is equal to $3U_{DC,4}$). In contrast to DCC the complementary switch pairs in CCC are $S_{1}\text{'}, S_{2}\text{'}, S_{3}\text{'}, \ldots , S_{n}\text{'}. Turning switches on allows connecting relevant clamping capacitors in series, what can generate the multilevel output voltage. Current paths for different switching states are presented in Fig. 12a. In Fig. 12b one can observe the switching states and capacitor currents of one phase leg of CCC. A given voltage level can be obtained in many different states, e.g., $u_{A0} = U_{DC,4}$ can be generated by four states, 2-5.

Unlike diode-clamped converter this structure can produce output voltage in every switching state of $2^{n-1}$ possible states. As is stated in Fig. 12b the clamping capacitor voltages can be charged or discharged depending on switching state, output current value and its direction. Because there are few redundant switching states that can produce the same output voltage level these redundant switching states can be utilized to balance voltages of clamping capacitors.

**Fig. 10. Different arrangements (and names) of one phase leg of five level capacitor-clamped converter (CCC); (a) Flying capacitor converter. (b) Multicell converter [11]**

**Fig. 11. Three-phase five-level capacitor-clamped converter (CCC)**

Capacitor-clamped converter has to utilize different control strategy compared to DCC because there exist more switching states than in DCC counterpart. The most suitable control strategy that can balance all clamping capacitors [12] is phase-shifted carrier PWM within limits of load angles $-\pi/2 > \varphi > \pi/2$. It is presented later in this paper. Clamping capacitor voltages are self-balanced, what means that any disturbance that can occur to these voltages will be lessened with time. The number of levels does not influence
on balancing capacitor voltages. As is stated in [12], the time constant describing voltage regain depends on capacitance of clamping capacitors, modulation index, load impedance and load angle. The most important fact is that, the greater load angle the longer time is needed to regain capacitor voltages. For load angles equal \( \pm \pi/2 \), this time constant is infinity. In other words it could be stated that CCC cannot operate with output current angles shifted by \( \pm \pi/2 \) with regard to output voltage what means that operation of CCC as reactive power compensator is not allowed. This is the main drawback of the CCC. The steady state behavior of the converter with load angle of 1.26, under phase-shifted carrier PWM is depicted in Fig. 13.

![Fig.13. Balanced output voltage \( u_{A0} \) of five-level capacitor-clamped converter (Fig. 9) with phase-shifted carrier method. (simulation carried out with \( R = 10 \Omega \), \( L = 100 \text{ mH} \), \( C = 1 \text{ mF} \), \( f_m = 50 \text{ Hz} \), \( U_{DC} = 200 \text{ V} \)](image)

**Cascaded converter with separate DC sources (CMC)**

The third type of multilevel converter is cascaded one with separate DC sources. The topology is given in Fig. 14 where DC sources can be connected to each other in series through two-level converters.

The \( n \)-level converter needs to use \((n-1)/2\) separate DC sources. Five-level converter with two separate sources and its output voltage waveform and current paths is presented in Fig. 15. Each voltage level numbered from 1 to 6 corresponds to exact state of all converter switches. Current paths give information about conducting switches for both current directions.

The CMC needs to use separate DC sources what means that for PCS application it is demanded to use multiple winding transformer that can produce separate voltages. It results in stable voltage of each level. The topology is also bulky like DCC with capacitor stabilized voltages since transformer has to be used.

The topology is the most promising for automotive applications and in energy systems that use alternative energy sources such as photovoltaic batteries or fuel cells is cascaded multicell converter [3], [7] or even SMES.

Cascaded inverters with capacitors can operate only for reactive loads (or for active power filtering where no real power is demanded).

Concluding, the topology also does not meet demands assumed for PCS, because transformers are needed.

![Fig.14. Three-phase five-level cascaded converter with separate DC sources](image)

![Fig.15. One phase leg of five-level cascaded multicell converter (CMC). (a) Structure. (b) current paths. (c) Output voltage waveform](image)

**Control strategies**

The control strategies are discussed briefly since there is only one that is suitable for PCS.

There are four main control strategies applied to multilevel converters [3] divided into two groups:

i) fundamental switching frequency, FSFM [6], [7],
   - selective harmonic elimination, SHE,
   - space vector control, SVC [10].

ii) higher switching frequency, HSF-PWM [8], [9],
   - sinusoidal pulse width modulation, SPWM,
   - space vector pulse width modulation, SVPWM.
Analysis of control strategies results in conclusion that SVC and SVPWM are the best solutions for PCS application. SVC is applicable for higher number of levels but SVPWM is more suitable for small number of levels.

**Space vector pulse width modulation (SVPWM)**

The method can be described using Fig. 16. This modulation method is similar to SVPWM of two-level inverter but the number of values of space vector depends on the number of output voltage levels and is much higher than in two-level one. The needed vector is synthesized by averaging adjacent three vectors. Its value is taken from a certain triangle, such as depicted in Fig. 16. All possible vectors are indicated in this figure. It is necessary to add that the given vector can be produced in several switching states.

This control strategy has following advantages [3]: allows balancing of capacitor voltages, results in low current ripple, permits for relatively easy hardware implementation by a digital signal processor.

**Comments on power part of multilevel converters**

Summing up all mentioned features can be seen that first mentioned topology DCC has following advantages and following disadvantages:

Advantages of this topology are i) only \( n \)-1 bulky capacitors are used, ii) reactive power can be controlled. Disadvantages are i) keeping capacitor voltages at certain level for converter with \( n > 3 \) is difficult, ii) many diodes are used.

The second topology CCC presents more interesting features and it has following advantages: i) there is no problem of unbalanced capacitor voltages, ii) reactive and real power flow can be controlled, iii) many capacitor has additional energy that can be used for occurred faults (outages) in the mins. Disadvantages are i) great number of bulky and costly capacitors, ii) complex control needed when measuring of capacitor voltages exists.

Third topology CMC uses separate DC sources what is the major drawback in PCS application because it needs to use heavy multiple winding transformer. Although CMC is very promising topology for other applications and it needs the smallest number of parts it was not taken into consideration for choosing the multilevel converter for power conditioning system.

The first topology, although has unbalanced voltage problem, can operate in PCS application by using back-to-back connection. In that case AC-DC converter is composed of three phase-legs and DC-DC converter consists two phase-legs.

Authors deem CCC as the most fitted converter topology to PCS. This choice was dictated by self-balancing property and greater freedom of selecting proper switching state.

**Conclusions**

1. Selecting the best multilevel topology is difficult because all three topology has different advantages and drawbacks when are used in PCS. These features are observed only at particular operation modes what shows that there is no one that is the best solution for PCS.
2. Nevertheless the three-level diode-clamped converter with space vector pulse width modulation (SVPWM) is the best candidate for AC-DC converter for PCS with SMES. The PCS system has to operate as UPS of high dynamics, reactive power compensator and as active power filter.
3. The DC-DC converter has to be two-level one because the shape of the DC voltage of SMES is to be \( \pm U_{dc} \).
4. The possibility of application of capacitor-clamped converter (especially with \( n > 3 \)) has to be thoroughly examined from the point of view of application in PCS.

**Remark**

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**REFERENCES**